



DM648 Evaluation Module

Technical Reference Guide

August, 2007

Revision history

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0.1	May, 2007	Preliminary version.
0.2	August, 2007	Made minor modifications to preliminary contents.

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PRELIMINARY

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Introduction

Congratulations on the purchase of the DM648 Evaluation Module (EVM).

Outstanding features and potential applications

The DM648 EVM is the first in a series of solutions designed for Texas Instruments' TMS320DM648 digital signal processors (DSPs), which offer developers significant performance enhancements and price benefits over previous generations of DSPs. DSPs also give developers significantly more programmability and flexibility than other processor options — such as FPGAs and ASSPs — that are too rigid for complex, evolving video systems. The module, developed by Lyrtech, provides hardware and driver software ideal for the efficient development of multichannel video security systems, digital video recording and high-performance imaging.

With the performance improvements and highly differentiated functionalities offered by Texas Instruments' DM648 DSPs, the EVM allow developers to create sophisticated video systems with increased simultaneous multichannel processing and lower per-channel costs. The DM648 EVM is equipped with eight standard-definition video inputs coupled with eight channels for audio recording, two 1-Gbps Ethernet ports for high-speed connectivity to a video server, and a high-definition video input for critical high-resolution video, making the system optimal for high-performance video applications.

Document organization

This document is organized as follows:

[Hardware overview](#) presents the major hardware elements of the product, including connectors and various other components of the module.

[Specifications](#) outlines the major specifications of the DM648 EVM.

Conventions

In a procedure containing several steps, the operations that the user has to execute are numbered (1, 2, 3...). The diamond (◆) is used to indicate a procedure containing only one step, or secondary steps. Lowercase letters (a, b, c...) can also be used to indicate secondary steps in a complex procedure.

The abbreviation *NC* is used to indicate no connection.

Capitals are used to identify any term marked as is on an instrument, such as the names of connectors, buttons, indicator lights, etc. Capitals are also used to identify key names of the computer keyboard.

All terms used in software, such as the names of menus, commands, dialog boxes, text boxes, and options, are presented in **bold** font style.

The abbreviation *N/A* is used to indicate something that is not applicable or not available at the time of press.

Note

The screen captures in this document are taken from the software version available at the time of press. For this reason, they may differ slightly from what appears on your screen, depending on the software version that you are using. Furthermore, the screen captures may differ from what appears on your screen if you use different appearance settings.

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PRELIMINARY

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Hardware overview

This chapter presents an overview the DM648 EVM by describing its parts and functions.

DM648 EVM block diagram

The DM648 EVM can be represented by the following block diagram:

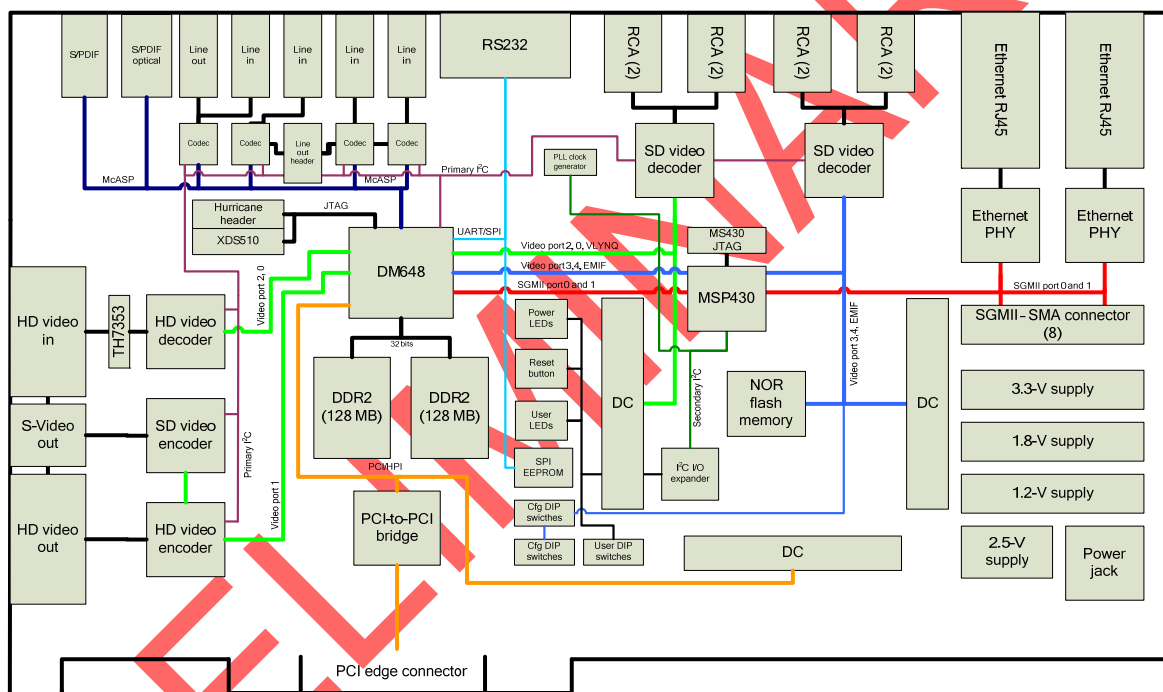


Figure 1 DM648 EVM block diagram

DM648 EVM parts and functions

Physically, the EVM is laid out as follows:

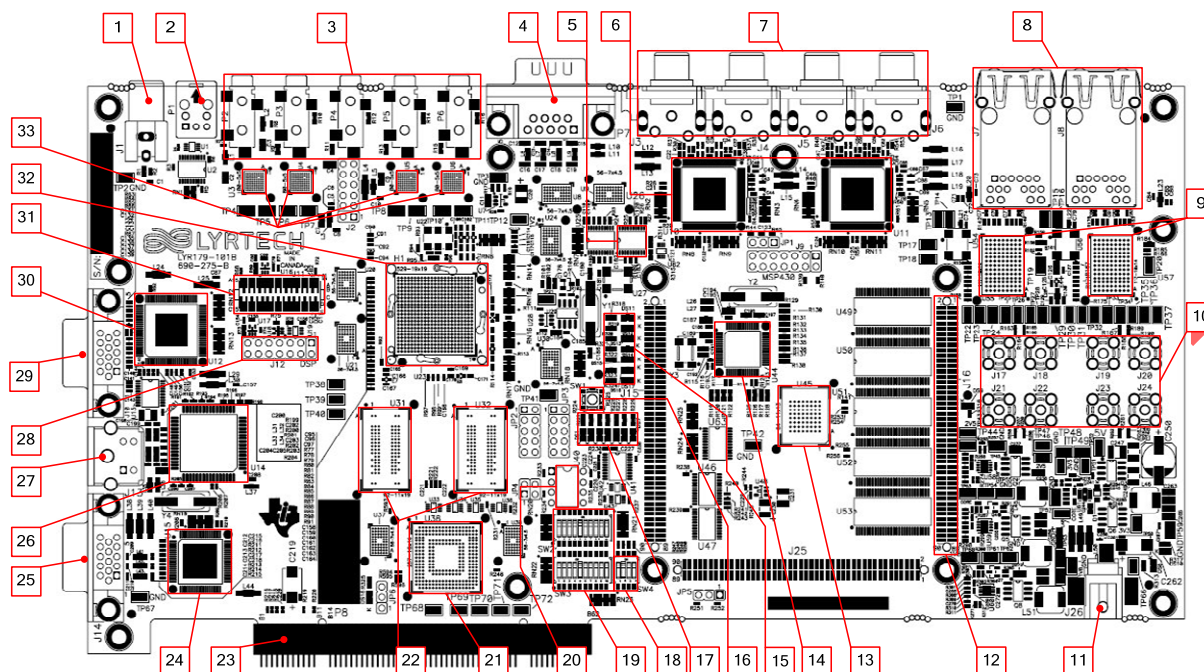


Figure 2 DM648 EVM layout

1. Digital audio connector

Standard RCA connector following the S/PDIF protocol specifications.

Note

Prior to using a digital output, the software must enable the feature by communicating with the MSP430 microcontroller. The digital output is taken from the McASP serializer 7 (AXR7). See [McASP multiplexer](#) for details.

2. Digital optical audio connector

Standard TOSLINK connector following the S/PDIF protocol specifications.

Note

Prior to using a digital output, the software must enable the feature by communicating with the MSP430 microcontroller. The digital output is taken from the McASP serializer 7 (AXR7). See [McASP multiplexer](#) for details.

3. Line connectors

Standard 1/8" audio jacks. There are five connectors — the first on the left (as illustrated above) is a line out connector, while the remaining four connectors are line in.

4. RS232 connector

Standard series communications connector.

5. PLL clock synthesizer

The CDCE906 is one of the smallest and powerful PLL synthesizer/multiplier/divider available today. However, despite its small physical outlines, the CDCE906 remains very flexible, generating precise video (27 MHz or 54 MHz) and audio system clocks from multiple sampling frequencies ($f_s = 16$ kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz) and accepting crystal frequencies from 8 MHz up to 54 MHz.

The PLL clock synthesizer generates the CLKIN1 (core clock reference), CLKIN2 (DDR2 SDRAM clock reference), and the HD, SD, module reference, and codec clocks. The CDCE906 can use the onboard 27-MHz oscillator or the VCXO (PI6CX100-27 W or compatible) as source for audio/video synchronization.

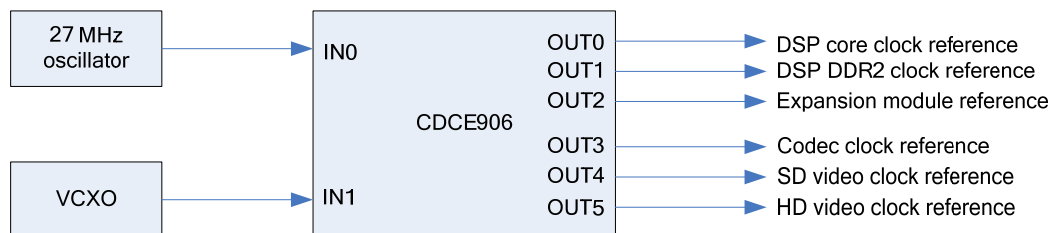


Figure 3 Clocks

6. Standard-definition video decoders

The TVP5154 device is a 4-channel, low-power, NTSC/PAL/SECAM video decoder. The DM648 EVM is equipped with two such devices. The first TVP5154 (channels 1–4) is connected on the video ports 0 and 2 of the DSP. The second TVP5154 (channels 5–8) is connected to video ports 3 and 4.

Each channel of the TVP5154 decoder converts NTSC, PAL, or SECAM video signals to 8-bit ITU-R BT.656 format. All four channels of the TVP5154 are independently controllable. The decoders share one crystal for all channels and for all supported standards. The TVP5154 can be programmed using a single inter-integrated circuit (I²C) serial interface. The decoder uses a 1.8-V supply for its analog and digital supplies, and a 3.3-V supply for its I/O. The optimized architecture of the TVP5154 decoder allows for low power consumption.

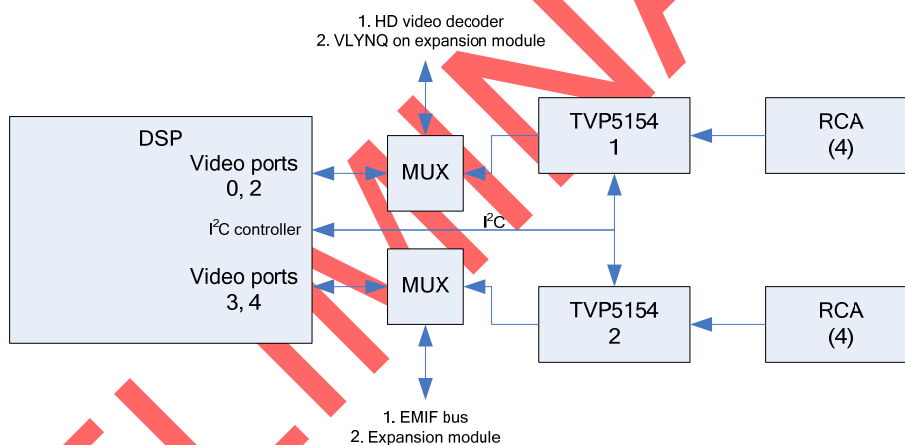


Figure 4 SD video decoder configuration

7. RCA video connectors

Eight RCA input connectors for standard definition video. Video channels are numbered 1 to 8, as illustrated here.

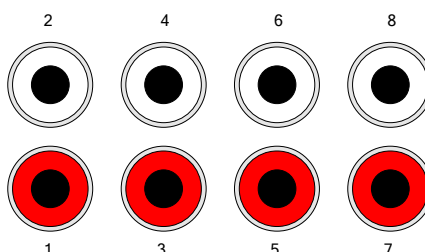


Figure 5 Video channel order

8. RJ45 Ethernet connectors

Shielded 10Base-T, 100Base-TX, 1000Base-T (Gigabit) Ethernet connectors capable of, respectively, 10 Mbps, 100 Mbps, and 1000 Mbps. These connectors are used to connect the platform to your computer using standard Gigabit Ethernet cables.

9. Ethernet PHYs

The platform is equipped with two Marvell 88E1111-2 PHYs. These PHYs are the lowest power, smallest form factor, highest performance, and highest port density solutions in volume production. The device performs all the physical layer (PHY) functions for half-duplex and full-duplex 10Base-T Ethernet on CAT 3, CAT 4, and CAT 5 cable, and half-duplex and full-duplex 100Base-TX and 1000Base-T Ethernet on CAT 5 twisted pair cable.

10. SMA connectors

These eight connectors can be connected to the serial Gigabit media-independent interface (SGMII) of the DSP, allowing direct communications with the DSP. For details, see [Ethernet](#).

11. Power connector

This connector is used to connect the +5 V DC universal power supply included with the DM648 EVM.

12. Module expansion connectors

The DM648 EVM is equipped with three SAMTEC SFM-145-L2-S-D-A expansion connectors for user expansion module needs. For details about the pin assignments, see [Module expansion connectors](#).

13. NOR flash memory

256-Mb Spansion S29GL256N flash memory with a 16-bit data bus is connected to the EMIFA interface and used to store parameters, applications, *etc.*

The ready signal from the flash memory is not connected to the DSP ARDY pin of the DSP, so the wait state can only be performed by an internal DSP wait state.

Note

Before using the flash memory, make sure that the VP[3-4]/EMIFA multiplexer is in the correct direction.

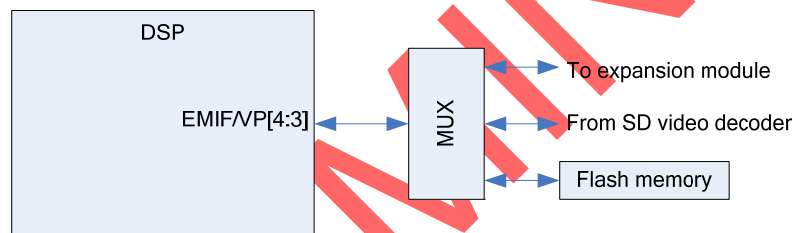


Figure 6 Flash memory configuration

14. MSP430-series microcontroller

The microcontroller oversees such tasks as DSP resets and power sequencing startup. Some of the platform peripherals are also directly connected to the microcontroller, placing them under its direct control. The MSP430 microcontroller supervises:

- PLL clock synthesizer
- I²C expander for the LEDs and user DIP switches
- Mux control
- DM648 EVM reset
- Power supply control

15. Power LEDs

16. Reset button

This button is used to reset the DSP of the DM648 EVM.

17. LEDs

Series of seven LEDs controlled by the DSP. The following signals are connected to the LEDs:

Table 1 Signals connected to the DM648 EVM/DVDP LEDs

LED	Signal	Description
DS1–6	N/A	User defined.
DS7	VCC_MSP430_3V3	MSP430 3.3 V power supply signal.

18. User DIP switches

Identified SW2 and SW3 on the silkscreen, the platform is equipped with two banks of ten user-defined DIP switches. The following tables indicate the DIP switches' default configuration at startup (when the EVM is turned on).

Table 2 SW2 DIP switches

Switch	Boot mode signal	Description
SW2-[4-1]	BOOTMODE[3-0]	Boot mode selection.
SW2-5	LENDIAN	Little Endian.
SW2-6	HPIWIDTH	Host port interface data width.
SW2-7	AECLKINSEL	AECLKIN selection.
SW2-8	PCI66	Set PCI but to support 66 MHz.
SW2-[10-9]	UNUSED	Reserved for future use.

Table 3 SW3 DIP switches

Switch	Boot mode signal	Description
SW3-1	PLLBYPASS2	PLL2 bypass mode (DDR2 clock).
SW3-2	DVREN	TBD.
SW3-3	FASTBOOT	Fast boot.
SW3-4	EMIFBWIDTH	EMIFB width.
SW3-5	HPI_EN	Host port interface enable.
SW3-6	UART/SPI _{in}	UART or SPI enable.
SW3-7	DC_GPIO5	Directly connected to module expansion connectors.
SW3-8	ALT_BOOT	Alternate boot mode.
SW3-[10-9]	UNUSED	Reserved for future use.

19. DSP configuration DIP switches

Marked SW4 on the silkscreen, this bank of four DIP switches is used to software configure the DSP.

20. SPI EEPROM

This EEPROM, accessible from the DSP through an SPI port, allows users to store data (*e.g.* bootable application or parameters).

21. PCI-to-PCI bridge

Texas Instruments PCI2060. The PCI2060 is a 32-bit, asynchronous, PCI-to-PCI bridge. The PCI2060 makes it possible for the primary and secondary bus clocks to be completely asynchronous. It also supports PCI clock frequencies up to 66 MHz. See [PCI bus](#) for more.

22. DDR2 SDRAM

Two 128-MB Micron MT64M16 or compatible devices of DDR2 SDRAM (total: 256 MB). The clock frequency is 250 MHz, allowing data rates of 2 GBps.

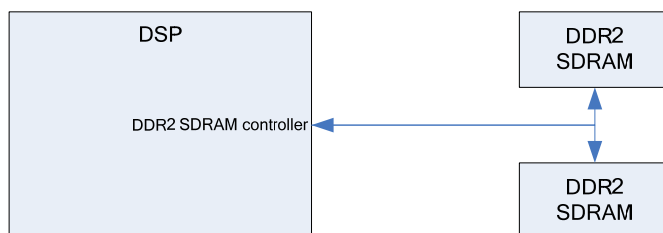


Figure 7 DDR2 SDRAM configuration

23. Universal PCI edge connector

This type of PCI edge connector allows connecting the platform in 3.3-V and 5-V PCI slot.

24. High-definition video encoder

Texas Instruments THS8200. The THS8200 is a complete video back-end D/A solution for systems requiring digital component video signal conversion into the analog domain. The THS8200 accepts a variety of digital input formats (4:4:4 and 4:2:2 formats), over a 3×10 -bit, 2×10 -bit, or 1×10 -bit interface.

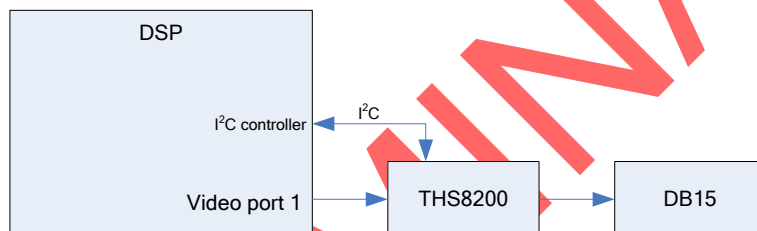


Figure 8 HD video encoder configuration

25. High-definition video output connector

Standard VGA DB15 connector to output of high-definition video.

Table 4 HD video output DB15 connector pin assignments

Pin	Signal	Pin	Signal
1	Red video/Pr signal	9	NC
2	Green video/Y signal	10	Sync ground return
3	Blue video/Pb signal	11	NC
4	NC	12	NC
5	Ground A	13	HSYNC
6	Red/Pr ground return	14	VSYSNC
7	Green/Y ground return	15	NC
8	Blue/Pb ground return		

26. Standard-definition video encoder

Philips SAA7105H. The SAA7105H is an advanced video encoder that converts 1280×1024 resolution digital video data to PAL (50 Hz) or NTSC (60 Hz) video signals. A programmable scaler and anti-flicker filter (maximum five lines) ensures properly sized and flicker-free television display as CVBS or S-Video output.

The SAA7105 input port is connected to the THS8200 (24, above) auxiliary port to share video port 1 of the DSP, implying that standard-definition and high-definition video are mutually exclusive. The standard-definition video encoder is accessible from the S-Video connector (below).

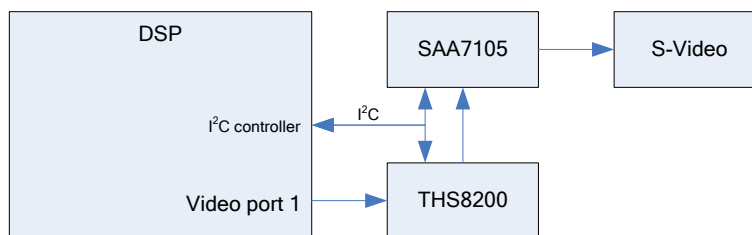


Figure 9 SD video encoder configuration

27. S-Video output connector

Standard mini-DIN, 4-pin connector used to output S-Video signals.

28. XDS510-compatible JTAG header

JTAG header compatible with Texas Instruments XDS510-class emulators used in DSP emulation.

29. High-definition video input connector

Standard VGA DB15 connector to input high-definition video.

Table 5 HD video input DB15 connector pin assignments

Pin	Signal	Pin	Signal
1	Red video	9	NC
2	Green video	10	Sync ground return
3	Blue video	11	NC
4	NC	12	NC
5	Ground A	13	HSYNC
6	Red ground return	14	VSYNC
7	Green ground return	15	NC
8	Blue ground return		

30. High-definition video decoders

Texas Instruments TVP7000 (2×). The TVP7000 is a complete solution for digitizing video and graphic signals in the RGB or YPbPr color spaces. The device supports pixel rates up to 150 MHz, making it easy to use for computer graphic digitizing up to the VESA standard of SXGA resolution (1280 × 1024 pixels) at 75 Hz screen refresh rate, and in video environments for digitizing digital television formats, including HDTV up to 1080 p. The TVP7000 can be used to digitize CVBS and S-Video signals with 10-bit ADCs.

To improve and also increase the flexibility of this input, THS7353 video filters are added between the high-definition input connectors (above) and the TVP7000. Only RGB are routed to the filter, the HSYNC and VSYNC signals are routed directly to the TVP7000 decoder.

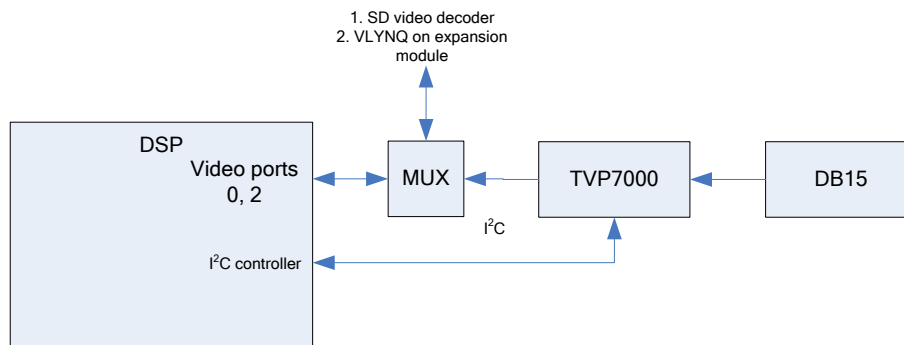


Figure 10 HD video decoder configuration

31. Hurricane JTAG header

60-pin JTAG header, part of a new generation of JTAG. This header supports existing JTAG scans, multiprocessor breakpoints, and HS RTDX capabilities, as well as being equipped with additional EMU pins for advanced emulation features.

32. TMS320DM648 DSP

The DM648 DSP is part of Texas Instruments' highest-performance fixed-point DSP family, the TMS320C64x+. The device is based on the third-generation, high-performance, advanced VelociTI very-long-instruction-word (VLIW) architecture developed by Texas Instruments, making them ideally suited to digital media applications. These C64x+ DSPs support added functionality and have an expanded instruction set from previous devices.

With performances of up to 7200 million instructions per second (MIPS) at a clock rate of 900 MHz, the C64x+ core of the DM647/DM648 DSPs offers solutions to high-performance digital signal processing programming challenges. The C64x+ core possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. For details about the DSP, see [DSP](#).

33. Audio codecs

Texas Instruments TLV320AIC33 (4x). The TLV320AIC33 is a low-power, stereo audio codec with stereo headphone amplifier, and multiple inputs and outputs programmable in single-ended or fully differential configurations. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 14 mW from a 3.3-V analog supply.

All four stereo inputs are accessible through onboard 1/8" stereo jacks (3) and outputs are available on a 1/8" stereo jack (3). All stereo outputs are also accessible from the J2 header.

Table 6 Audio codec output signals on J2

Pin no.	Signal	Pin no.	Signal
1	AUD_OUT5	2	AUD_OUT1
3	GNDA	4	GNDA
5	AUD_OUT6	6	AUD_OUT2
7	AUD_OUT7	8	AUD_OUT3
9	GNDA	10	GNDA
11	AUD_OUT8	12	AUD_OUT4

DSP

The DSP of the DM648 EVM is a TMS320CDM648. This section presents this device in more detail.

DSP reset

The reset is controlled by the MSP430 microcontroller. When the module is turned on, the MSP430 verifies all the power supply rails and deasserts the DSP reset, at which time the DSP latches the configuration switches.

Memory map

For details about the TMS320DM648 memory map, refer to its specifications sheet from Texas Instruments.

UART/SPI

The UART and SPI EEPROM use the same DSP signals. DIP switch SW3-6 is used to enable/disable the UART and SPI. The UART is directly connected to an RS232 transceiver, but only TX, RX CTS, and RTS are used. The RS232 is available on a DB9 connector. See [4](#), above.

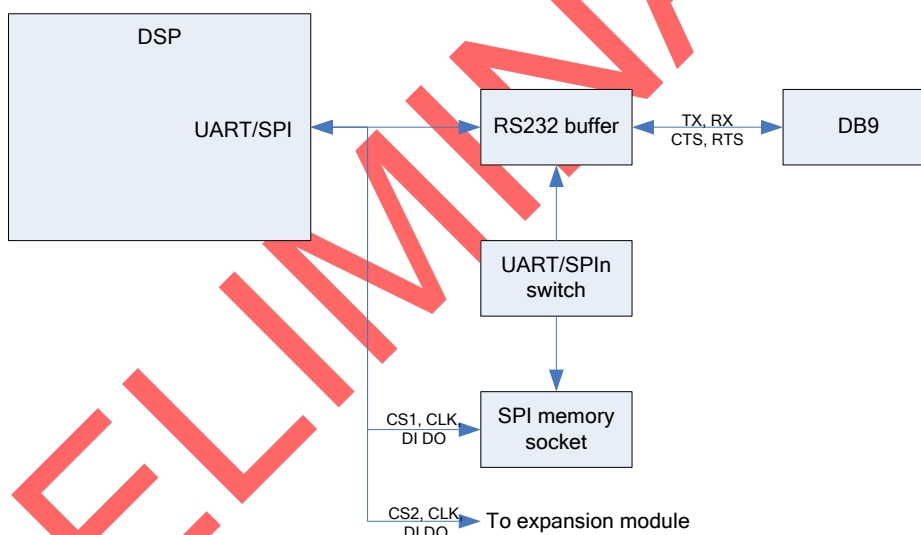


Figure 11 UART/SPI configuration

Video ports 0 and 2

Video port 0 is used to interface the high-definition video input and standard video inputs (channels 1–2). Video port 2 is multiplexed with standard video inputs (channels 3–4) and VLYNQ.

Video port 1

Video port 1 is used to interface the standard (S-Video) and high-definition video outputs.

Video ports 3 and 4

Video ports 3 and 4 are multiplexed with the EMIFA bus. Video ports 3 and 4 are used for standard video inputs (channels 5–8).

SGMII ports

The SGMII ports are directly connected to the Ethernet PHY. For details, see [Ethernet](#).

Timer ports

The timer ports of the DSP are directly connected to the MSP430 microcontroller or the module expansion connector (J15). Timer port 0 is connected to the MSP430 microcontroller and timer port 1 is connected to the module expansion connector.

Primary I²C bus

The primary I²C bus is used to control the majority of I/O components. The primary I²C bus is also accessible from a header (JP2 and JP3) and from module expansion connector J15.

There are also jumpers (JP4) to disconnect the DSP from the primary I²C bus. The jumpers must be placed between 1-2 for SDA and 3-4 for SCL.

Table 7 Primary I²C bus memory map by address

I ² C address (hexadecimal)	Description of the memory block
0x00	DM648 — DM648 DSP Note The DM648 DSP default address is 0x00, but it can be modified by software.
0x18	TLV320AIC33 — Analog audio channels 1 and 2.
0x19	TLV320AIC33 — Analog audio channels 3 and 4.
0x1A	TLV320AIC33 — Analog audio channels 5 and 6.
0x1B	TLV320AIC33 — Analog audio channels 7 and 8.
0x20	THS8200 — High-definition video decoder.
0x2C	THS7353 — High-definition input video filter.
0x44	SAA7105H — Standard definition video encoder.
0x5C	TVP7000 — High-definition video decoder.
0x5E	TVP5154 — Standard-definition video decoder channels 1–4.
0x5F	TVP5154 — Standard-definition video decoder channels 5–8.
0x70	MSP430 — DM648 EVM supervisor.

McASP

See [Audio](#) for details about the McASP.

PCI/HPI

See [PCI/HPI](#) for details about these interfaces.

Ethernet

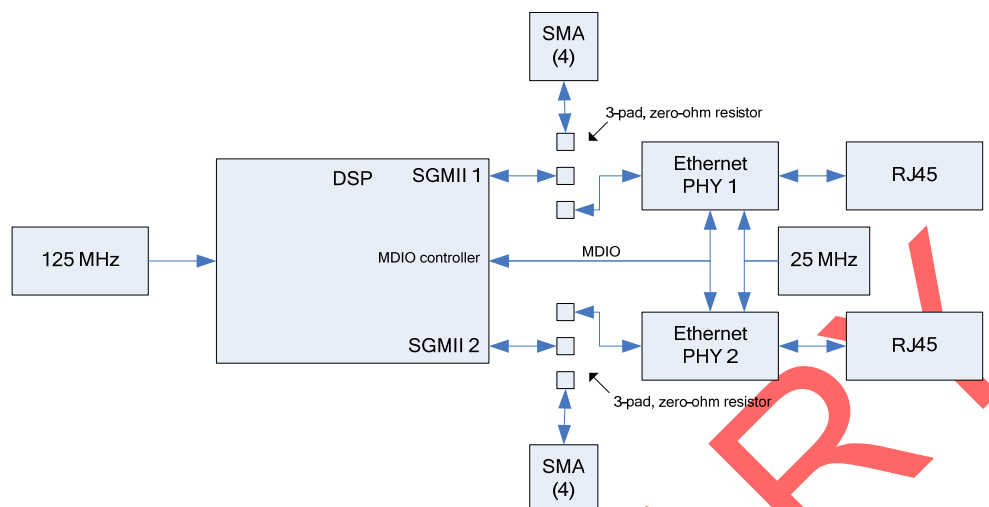


Figure 12 Ethernet section configuration

Ethernet PHYs

The DSP is designed with two independent SGMII that connect directly to the Ethernet PHYs of the DM648 EVM. The Ethernet PHYs are controlled through the DSP MDIO interface, making it possible to modify hardware defaults by software. The SGMII support 1-Gbps, 100-Mbps, and 10-Mbps links.

To connect the Ethernet PHYs to a LAN, two RJ45 Ethernet connectors are used. See [DM648 EVM parts and functions](#) at position 8).

SMA connectors

The SGMII of the DSP can be disconnected from the PHYs and replaced by the SMA connectors of the DM648 EVM located in position 10 in [DM648 EVM parts and functions](#). Contact Texas Instruments for details.

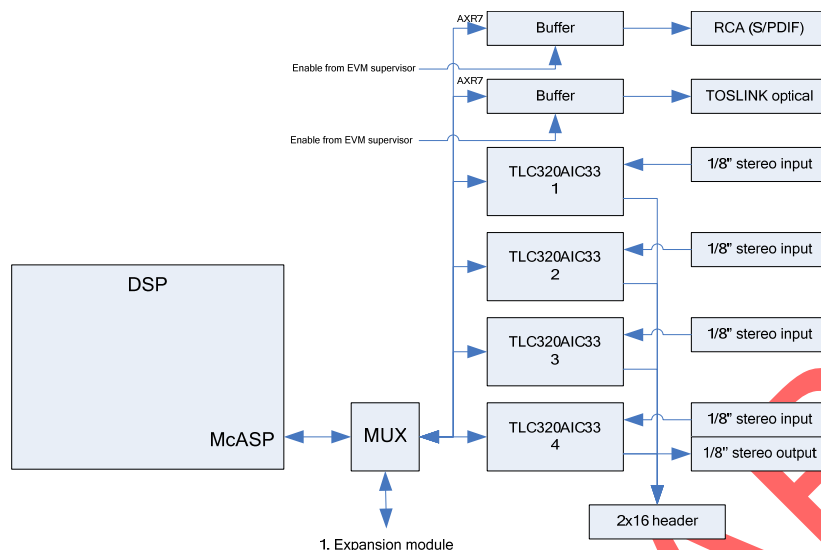


Figure 13 Audio section configuration

McASP multiplexer

The McASP multiplexer may be routed to the audio codec or to the module expansion connector by setting the mux (74CBT3T16212) to the proper settings through the MSP430 microcontroller.

PCI/HPI

PCI bus

The PCI-to-PCI bridge of the DM648 EVM (21 in [DM648 EVM parts and functions](#)) is used to decouple the onboard PCI bus from the PCI bus of the host device. The PCI-to-PCI bridge supports 3.3 V and 5 V PCI signaling. Note that on some older or lower-quality computers, 5-V slots do not allow the 3.3-V power pins of PCI connectors to be connected. For this reasons the PCI-to-PCI bridge uses 3.3-V PCI to supply its core. JP6 was added so that the PCI can be powered from 3.3-V PCI or the generated 3.3 V with onboard power supply. JP6 in position 1–2 uses 3.3 V PCI and in position 2–3 uses the onboard 3.3 V. LED DS18 was added to more easily troubleshoot the absence of 3.3 V.

The primary PCI bus is to one from the universal PCI edge connector to the PCI-to-PCI bridge, the secondary is the one between the PCI-to-PCI bridge, DSP, and expansion module connector (see [DM648 EVM block diagram](#)). When the DM648 EVM is not in a PCI slot (automatic detection), the PCI-to-PCI bridge is left unpowered (in which case you must place JP6 in the 1–2 position. Failing to do so may damage the PCI-to-PCI bridge) and the secondary bus is disconnected from the PCI-to-PCI bridge by a FET switch (U37 and U39). The secondary bus can be still used by a PCI master board through the expansion module connectors (J25). The PCI-to-PCI bridge supports up to 2 additional PCI bus masters (the DSP is the third PCI bus master).

WARNING

When the DM648 EVM is connected to a PCI slot, do not power the board from the DC input jack. The necessary 5 V is drawn from the PCI slot. Doing so may result in serious damage or injury.

Host port interface

When the DM648 EVM is not used in PCI bus mode, it can be used in HPI mode, instead. You can switch modes with Dpi switch SW3-5. Whatever the position of the DM648 EVM (in a PCI slot or not), the DSP HPI may still be accessed from an expansion module.

Module expansion connectors

Table 8 Module expansion connector pin assignments (J15)

Pin no.	Signal	Pin no.	Signal
1	0_CLKA	2	1_CLKA
3	GND	4	GND
5	0_CLKB	6	1_CLKB
7	0_FSA	8	1_FSA
9	GND	10	GND
11	0_FSB	12	1_FSB
13	0_TR0	14	1_TR0
15	GND	16	GND
17	0_TR1	18	1_TR1
19	0_TX0	20	1_TX0
21	GND	22	GND
23	0_TX1	24	1_TX1
25	5 V	26	5 V
27	GND	28	GND
29	VP2_CTL0	30	VP2_CLK0
31	VP2_D2	32	VRXD0_VP2_D12
33	GND	34	GND
35	VP2_D3	36	VRXD1_VP2_D13
37	VP2_D4	38	VRXD2_VP2_D14
39	GND	40	GND
41	VP2_D5	42	VRXD3_VP2_D15
43	VP2_D6	44	VTXD0_VP2_D16
45	GND	46	GND
47	VP2_D7	48	VTXD1_VP2_D17
49	VP2_D8	50	VTXD2_VP2_D18
51	GND	52	GND
53	VP2_D9	54	VTXD3_VP2_D19
55	VP2_CTL1	56	VCLK_VP2_CLK1
57	GND	58	GND
59	3.3 V	60	VP2_CTL2_VSCRUNn
61	CLK	62	3.3 V
63	GND	64	GND
65	RESET_STATn	66	TOUT0

Pin no.	Signal
67	SYSCCLK4
69	GND
71	GPIO0
73	GPIO2
75	GND
77	GPIO4
79	SPI_DI
81	GND
83	SPI_CS2n
85	SPI_CLK
87	GND
89	3.3 V

Pin no.	Signal
68	TINP0
70	GND
72	GPIO1
74	GPIO3
76	GND
78	GPIO5
80	SPI_DO
82	GND
84	SCL
86	SDA
88	GND
90	3.3 V

Table 9 Module expansion connector pin assignments (J16)

Pin no.	Signal
1	3.3 V
3	GND
5	5 V
7	ASDWE _n /VP3_CTL0
9	GND
11	AED1/VP3_D3
13	AED3/VP3_D5
15	GND
17	AED5/VP3_D7
19	AED7/VP3_D9
21	GND
23	AECLKOUT/VP3_CLK1
25	AED8/VP3_D12
27	GND
29	AED10/VP3_D12
31	AED12/VP3_D16
33	GND
35	AED14/VP3_D18
37	ABA0/VP4_CTL0
39	GND
41	ABE0 _n /VP4_D2

Pin no.	Signal
2	3.3 V
4	GND
6	AECLK1/VP3_CLK0
8	AED0/VP3_D2
10	GND
12	AED2/VP3_D4
14	AED4/VP3_D6
16	GND
18	AED6/VP3_D8
20	AR _n W/VP3_CTL1
22	GND
24	AOE _n /VP3_CTL2
26	AED9/VP3_D13
28	GND
30	AED11/VP3_D15
32	AED13/VP3_D17
34	GND
36	AED15/VP3_D19
38	AARDY/VP4_CLK0
40	GND
42	ABE1 _n /VP4_D3

Pin no.	Signal	Pin no.	Signal
43	AEA10/VP4_D4	44	VP4_D5
45	GND	46	GND
47	ACE2n/VP4_D6	48	ACE3n/VP4_D7
49	AEA0/VP4_D8	50	AEA1/VP4_D9
51	GND	52	GND
53	ABA1/VP4_CTL1	54	VCLK/VP4_CLK1
55	AADS _n /VP4_CTL2	56	AEA2/VP4_D12
57	GND	58	GND
59	AEA3/VP4_D13	60	AEA4/VP4_D14
61	AEA5/VP4_D15	62	AEA6/VP4_D16
63	GND	64	GND
65	AEA7/VP4_D17	66	AEA8/VP4_D18
67	AEA9/VP4_D19	68	AEA11
69	GND	70	GND
71	AEA12	72	AEA13
73	AEA14	74	AEA15
75	GND	76	GND
77	AEA16	78	AEA17
79	AEA18	80	AEA19
81	GND	82	GND
83	AEA20	84	AEA21
85	AEA22	86	AEA23
87	GND	88	GND
89	3.3 V	90	3.3 V

Table 10 Module expansion connector pin assignments (J25)

Pin no.	Signal	Pin no.	Signal
1	S_CLKOUT1	2	S_CLKOUT2
3	GND	4	GND
5	S_CLKOUT3	6	PCLK/HHWIL
7	RST _n _GP01	8	NC
9	GND	10	GND
11	S_GNT1 _n	12	S_GNT2 _n
13	S_GNT3 _n	14	S_REQ1 _n
15	GND	16	GND
17	S_REQ2 _n	18	S_REQ3 _n

Pin no.	Signal
19	AD_HD_31
21	GND
23	AD_HD_29
25	AD_HD_27
27	GND
29	AD_HD_25
31	CBE3n/GP07
33	GND
35	AD_HD_23
37	AD_HD_21
39	GND
41	AD_HD_19
43	AD_HD_17
45	GND
47	CBE2n/HRWn
49	IRDYn/HRDYn
51	GND
53	DEVSELn/HCNTL1
55	S_LOCKn
57	GND
59	SERRn/HDS1n
61	CBE1/HDS2n
63	GND
65	AD_HD_14
67	AD_HD_12
69	GND
71	AD_HD_10
73	AD_HD_08
75	GND
77	AD_HD_07
79	AD_HD_05
81	GND
83	AD_HD_03
85	AD_HD_1
87	GND
89	INTAn

Pin no.	Signal
20	AD_HD_30
22	GND
24	AD_HD_28
26	AD_HD_26
28	GND
30	AD_HD_24
32	NC
34	GND
36	AD_HD_22
38	AD_HD_20
40	GND
42	AD_HD_18
44	AD_HD_16
46	GND
48	FRAMEEn/HINTn
50	TRDYn/GP05
52	GND
54	STOPn/HCNTL0
56	PERRn/HCSn
58	GND
60	PAR/HASn
62	AD_HD_15
64	GND
66	AD_HD_13
68	AD_HD_11
70	GND
72	AD_HD_09
74	CBE0n/GP04
76	GND
78	AD_HD_06
80	AD_HD_04
82	GND
84	AD_HD_02
86	AD_HD_00
88	GND
90	NC

MSP430 microcontroller — DM648 EVM supervisor

TBD.

PRELIMINARY

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Specifications

This chapter outlines the technical specifications of the DM648 EVM.

Note

The specifications in this chapter are subject to change without notice.

General specifications

- Mass: 277.3 g
- Length: 263.0 mm
- Width: 136.0 mm
- Height: 48.8 mm (feet included)
- Feet: 17.8 mm
- Operating temperature range: 0°C to 70°C (non-condensing)
- Storage temperature range: -55°C to 150°C (non-condensing)

DSP

- Model: Texas Instruments TMS320DM647/8
- CPU clock: 720 MHz
- Instruction rate: 5760 MIPS
- DDR2: 256 MB, 250 MHz (500 MHz data rate)

Troubleshooting ports

- XDS510 JTAG connector
- Hurricane JTAG connector

Memory

- 256-MB DDR2 SDRAM per DSP
- 32-MB flash memory
- TBD KB SPI EEPROM

Mezzanine communications interface

- Module expansion connectors (3×)

For details about the specifications of this custom mezzanine communications interface, contact [Lyrtech](#).

Ethernet

- Two independent ports
- 10, 100, 1000 Mbits/s

PCI interface

- Primary PCI bus: 32 bits, 66 MHz or 33 MHz
- Secondary PCI bus: 32 bits, 66 MHz or 33 MHz
- Secondary PCI bus supports up to three masters (the DSP being one)

PRELIMINARY

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CONTACT US FOR MORE INFORMATION AT:

Lyrtech Inc.
4495 Wilfrid-Hamel Blvd., Suite 100
Quebec City, Quebec G1P 2J7 CANADA

Phone: (1)(418) 877-4644 (International)
(1)(888) 922-4644
(Toll free USA and Canada)
Fax: (1)(418) 877-7710

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